

**PRELIMINARY DRAFT
Data Sheet**

**212B MAC-8
Single-Chip Microprocessor Package**

MAC-8 FEATURES

- CPU
- Powerful and extensive instruction set
- 8 and 16 Bit operations
- DC to 2.06 MHz clock (0 - 85°C)* ~~DC to 1.9 MHz clock (0 - 75°C ambient)*~~
- Low power consumption
- Split power supply for speed and TTL compatibility

The MAC-8 is a single chip, bus-structured general purpose microprocessor with an 8-bit data bus and a 16-bit address bus. This device is implemented, using a complementary MOS technology, logic elements are implemented using one of three circuit techniques : pseudo nMOS (with pMOS load devices), dynamic nMOS logic arrays and the familiar CMOS. An appropriate mix of these three techniques has yielded a functionally dense design while maintaining the low power and high speed objectives of 380mW typical power at a 2.06 MHz clock rate. The MAC-8 was designed with extensive addressing modes which offers a powerful and flexible instruction set. The memory byte and instruction time requirements of the modal instructions depend on the mode and not on the function itself. The MAC-8 requires a 12volt supply for internal circuitry and a 5volt supply for TTL compatibility on in/out pins.

*Characterization is presently being done to assure functional operation to -40°C

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TABLE I MAC-8 PIN DESCRIPTION

POWER SUPPLY PINS

VSS:	VSS is the circuit ground.
VDD:	VDD is the main voltage to the device.
VCC:	VCC is the voltage supply which provides TTL compatibility on I/O pins.

ADDRESS PINS

A0 to A15:	The MAC-8 addressable space consists of 65,536 locations used for both memory and I/O. The 16 address pins select the appropriate memory location or I/O port.
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DATA TRANSFER PINS

D0 to D7:	The 8-bit bi-directional data bus is used for data transfer to and from the device.
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CLOCK PINS

CLOCK

RESONATOR IN/OUT:	These two pins are used to connect an external resonator to the internal clock generator. The device may also be operated with an external clock signal applied to the clock resonator in pin.
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CLOCK OUT:	This is a TTL compatible clock signal generated by the MAC-8 which can be used to synchronize other devices to the microprocessor.
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OTHER OUTPUT PINS

MEMORY READ:	A read memory request is indicated by a low signal on this pin. The signal remains low until the end of a read cycle. It will however remain low on successive memory read cycles without returning to the high state at the end of each cycle.
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MEMORY WRITE:	A write memory request is indicated by a low signal on this pin. The signal is delayed from the beginning of the cycle. Even on successive write cycles this signal always returns to the high state at the end of each write cycle.
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STATUS

S0 to S2:	The three status pins indicate various internal states of the microprocessor (See Table III).
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DMA ACKNOWLEDGE:	A low signal is generated on this pin by the microprocessor to indicate that the address and data bus is free for use by the requesting device. All the MAC-8 address and data pins as well as the memory read and write pins are put in their high impedance state when this happens.
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OTHER INPUT PINS

INTERRUPT:

An external device requests an interrupt by applying a low signal on this pin. This request is latched in the last cycle of the current instruction. It is only latched if the interrupt enable condition is set. The microprocessor on granting an interrupt, stores the condition register and the program counter on the stack, clears the interrupt enable, then reads from hexadecimal address FFFF(acknowledges interrupt). The microprocessor then reads the data on the data bus and uses it as the lower half of the address to the interrupt handler routine, the upper half is forced to zero.(See Table II)

RESET:

A reset is requested by a low signal on the pin. This request is latched on the last cycle of the current instruction. The reset request is non-maskable. The microprocessor stores the condition register and program counter on the stack, clears the interrupt enable, then reads from address FFFF. The program counter is however forced to zero(See Table II).

DMA REQUEST:

A DMA request, activated by a low signal on this pin, is used by an external device to gain access to the data and address bus. The microprocessor examines the request at the end of each cycle. The request will be granted at the beginning of the next cycle except when the microprocessor is waiting for a slow device during a read or write operation.

DATA READY:

The data ready control is used to synchronize the microprocessor with slow memory devices. A low signal on this pin tells the microprocessor to wait until the memory is ready for data transfer on either a read or write operation.

Table II. INTERRUPT ADDRESSES

Function	Address(Hex)
Interrupt acknowledge	FFFF
Reset handler	0000
Interrupt handler	0000 < N ≤ 00FF
Illegal opcode(trap)	0008

Table III. STATUS ASSIGNMENTS

Function	Status(s2,s1,s0)
PC change	000
No reportable status	100
IR fetch, no condition reg.	001
Halt	101
RP change	010
SP change	110
IR fetch with condition reg.	011
Trap or trouble	111

MAC-8 DIP PINOUT



FUNCTION		PIN NUMBER
Address	a15	12
	a14	11
	a13	10
	a12	09
	a11	08
	a10	07
	a9	06
	a8	04
	a7	03
	a6	02
	a5	01
	a4	40
	a3	39
	a2	38
	a1	37
	a0	36
Data	d7	14
	d6	15
	d5	16
	d4	17
	d3	18
	d2	19
	d1	20
	d0	21
Memory read		22
Memory write		23
Data ready		35
DMA request		33
DMA acknowledge		34
Interrupt		24
Reset		25
Clock out		32
Resonator out		31
Resonator in		30
Status s2		27
Status s1		28
Status s0		29
Vcc		05
Vdd		26
Vss		13

OP CODE ASSIGNMENT

Hex	Function	Binary
01	Set condition register	00000001
03	Clear condition register	00000011
04	Pop stack to A register	00000100
05	Pop stack to condition register	00000101
06	Push A register to stack	00000110
07	Push condition register to stack	00000111
0C	Find left one	00001100
0D	Load stack pointer	00001101
0E	Count ones	00001110
20-23	Zero	001000xx
24-27	Negate	001001xx
28-2B	Increment, decrement	001010xx
2C-2F	Complement	001011xx
30-33	Shift arithmetically(L,R)	001100xx
34-37	Rotate 8(L,R)	001101xx
38-3B	Shift logical(L,R)	001110xx
3C-3F	Rotate 9(L,R)	001111xx
40	Short jump if false	01000000
41	Long jump if false	01000001
42	Bump register pointer(+)8 bytes	01000010
43	Bump register pointer(+)16 bytes	01000011
44	Pop stack to B register	01000100
45	Pop stack to register pointer	01000101
46	Push B register to stack	01000110
47	Push register pointer to stack	01000111
48	Short jump if true	01001000
49	Long jump if true	01001001
4A	Debump register pointer(-)8 bytes	01001010
4B	Debump register pointer(-)16 bytes	01001011
4C	Find left one, clear	01001100
4D	Load register pointer	01001101
52	Jump on register bit false	01010010
53	Jump on memory bit false	01010011
58	Unconditional short jump	01011000
59	Unconditional long jump	01011001
5A	Jump on register bit true	01011010
5B	Jump on memory bit true	01011011

xx-Any monadic mode number may be inserted here.

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Hex	Function	Binary
60	Zero B register	01100000
61	Call if false	01100001
62	Sign extend	01100010
64	Return if true	01100100
65	Return if false	01100101
66	Unconditional return	01100110
67	Return from interrupt	01100111
68	Increment,decrement(B register)	01101000
69	Call if true	01101001
6A	Swap bytes in B register	01101010
6D	Load register address	01101101
6F	Load address	01101111
73	Jump on memory bit false ++	01110011
75	Add A to B logical	01110101
78	Halt	01111000
79	Unconditional call	01111001
7B	Jump on memory bit true ++	01111011
7D	Add A to B arithmetically	01111101
7F	Nop	01111111
80-87	Move	10000xxx
88-8F	Xor	10001xxx
90-97	Or	10010xxx
98-9F	And	10011xxx
A0-A7	Subtract	10100xxx
A8-AF	Add	10101xxx
B0-B7	Compare	10110xxx
B8-BF	Test	10111xxx
C0-C7	Move 16	11000xxx
C8-CF	Xor 16	11001xxx
D0-D7	Or 16	11010xxx
D8-DF	And 16	11011xxx
E0-E7	Subtract 16	11100xxx
E8-EF	Add 16	11101xxx
F0-F7	Compare 16	11110xxx
FC	Test	11111100

++ - Post increment of address.

xxx - Any dyadic mode may be used here except mode 4. The memory-to-memory mode 4 can only be used for 8 bit instructions. In the case of mode 4, 8 bit instructions use the op code for the corresponding 16 bit instruction. The op codes for 8 bit instruction and mode 4 are not to be used.

Note1 - All other possible op codes not listed here are illegal and as a result will cause the microprocessor to trap(See Table III).

Note2 - More information on the op codes is contained in the MAC-8 Processor User's Manual.

ABSOLUTE MAXIMUM RATINGS

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DC CHARACTERISTICS				
11.4v < Vdd < 12.6v				
4.75v < Vcc < 5.25v				
0° C < T < 85° C				
SYM.	PARAMETER	CONDITIONS	MAX.	MIN.
Iol	Output sink current	Vout=0.5v Vout=0.4v	- -	2.0ma 1.6ma
Ioh	Output source current	Vout=3.2v	-	160ua
Il	Input leakage current	Vin=0v or 5.25v	400na	-400na
OI	Output leakage current	Vout=0v or 5.25v	400na	-400na
Idd	Vdd supply current	Freq=0 ALU on Freq=0 ALU off Freq=2.06MHz*	10ma 5ma 45ma	- - -
Icc	Vcc supply current		5ma	-
Vinh	Input one level		Vcc+.25v	1.8v
Vinl	Input zero level		0.8v	-.25v
Vckh	External clock high level		Vdd+.25v	.75xVdd
Vckl	External clock low level		.25xVdd	-.25v

*The maximum Idd at other frequencies can be calculated using the following expression: $I_{dd} = 10 + 17 \times \text{FREQ}(\text{MHz}) \text{mA}$.

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ELECTRICAL CHARACTERISTICS

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TIMING CHARACTERISTICS			
11.4v < V _{dd} < 12.6v			
4.75v < V _{cc} < 5.25v			
C-load = 25 pf			
0°C < T < 85°C			
SYM.	PARAMETER	MAXIMUM	MINIMUM
T _{in}	Clock in low	-	243ns
T' _{in}	Clock in high	-	243ns
T _{cl}	Clock in low to clock out low	230ns	-
T _{c2}	Clock in high to clock out high	290ns	-
T _{out}	Clock out low	(T _{in} +110ns or T _{in} +T' _{in} -400ns) ¹	T _{in} +10ns
T' _{out}	Clock out high	(T' _{in} -10ns or 3000ns) ²	(T' _{in} -110ns or 400ns) ²
T _{ac}	Clock out to address transition	-	0ns
T' _{ac}	Clock out to address valid	60ns	0ns
T _{crd}	Delay to change of read or status	85ns	-
T _{access}	Time allowed to access off chip memory	-	T _{in} +T' _{in} -150ns
T _{dh}	Data hold time	-	0ns
T _{cw}	Delay to memory write start	220ns	50ns
T _{wc}	Delay after memory write ends	125ns	5ns
T _{wp}	Memory write pulse width	-	T _{in} +T' _{in} -290ns

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SYM.	PARAMETER	MAXIMUM	MINIMUM
Twd	Time available to write to memory	-	$T_{in} + T'_{in} - 290ns$
Tw dh	Data valid to clock high	-	0ns
Tw ds	Data out delay	235ns	-
Tw dw	Data hold time	-	15ns
Tmracc	Time allowed for data ready in	-	$T_{in} - 100ns$
Tryh	Data ready hold time	-	0ns
Tis	Interrupt or reset setup time	-	80ns
Tih	Interrupt or reset hold time	-	200ns
Tdmas	DMA setup time	-	200ns
Tdmah	DMA hold time	-	0ns
Tdmak	DMA acknowledge delay (ON)	100ns	-110ns
Tdmax	DMA acknowledge delay (OFF)	100ns	-110ns
Tdma	Address delay in DMA (OFF)	160ns	-
Tdmaa	Address start to DMA address float	-	0ns
T'dma	Address delay in DMA mode (ON)	160ns	-
Tr,Tf	Rise and fall times	1.0ns/pf	-
C _i	Input capacitance	10pf	-

1-Whichever is greater.
2-Whichever is less.

